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MODELLING AND DESIGN OF MUGFETS

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1. INTRODUCTION

CMOS technology has been proven as one of the most important achievements in modern engineering history. In less than 30 years, it has become the primary engine driving the world economy. The secret to the success is very simple: keep delivering more functionality with fewer resources. Device scaling makes this possible. For decades, progress in device scaling has followed an exponential curve: device density on a microprocessor doubles every three years

This forecast *promises* us another ten years of brightness. Scaling beyond 30 nm, however, can be much more difficult and different. Remember, we are quite close to the fundamental limits of semiconductor physics. . Device simulation requires new theory and approaches to help us understand device physics and to design devices at the sub-30nm scale. Efforts have been put forth in recent years [3-7], but much more is needed. For these purposes, we started a research project in 1997, the results of which make up this thesis.

1.1 SCALING DEVICES TO THEIR LIMITS

There are two primary device structures that have being widely studied and used in CMOS technology. One is the bulk structure, where a transistor is directly fabricated on the semiconductor substrate. The other one is called SOI (silicon-on-insulator), where a transistor is built on a thin silicon layer, which is separated from the substrate by a layer of insulator. The bulk structure is relatively simple from a device process point of view, and it is still the standard structure in almost all CMOS based products until this day.

For device scaling, we basically try to balance two things: device functionality and device reliability. Both of them have to be maintained at a smaller dimensional size. To accomplish this, we need to suppress any dimension voltage (V_{TH}) variations versus channel length, typically V_{TH} roll-off at shorter channel lengths.

1.2 DOUBLE GATE MOSFETS

All recent studies of alternative CMOS device structures have reached one common conclusion: the double-gate (DG) device design is ideally suited for ultimate CMOS scaling. A double-gate device structure is composed of a thin Si body (thinner than one half of the gate length) sandwiched between gate stacks (gate contact and gate dielectric). Three different double-gate structures are most commonly used. They are: 1) planar double-gate device, 2) vertical surround-gate device, and 3) FinFet (with a fin-shaped body) [4, 23, 29-31]. Double-gate structures have exhibited numerous advantages over conventional bulk device structures. The presence of two gates significantly reduces short

channel effects, improves punch-through properties, permits complete dielectric isolation and reduces junction capacitance [4, 32]. In addition, thin body double-gate MOSFETs also provide nearly ideal sub-threshold slope. The reduced junction capacitance and presence of two channels drastically boosts the speed and drive current of double-gate device structures.

2. THEORETICAL METHODLOGY

2.1 POTENTIAL PROFILE

Fig. shows typical distributions of the conduction band edge along the transistor length. Since the two MOSFET species under analysis are depleted at different gate voltages V_g, we have plotted them for approximately the same value of the drain current to provide a more fair comparison. One can see that the potential profiles in both cases are very similar, with the exception that the sensitivity of the potential peak to gate voltage is approximately twice stronger for the double-gate transistor. In the single-gate device the electrostatic potential changes almost linearly between the gate and the ground electrodes, with half V_g being in the center of the channel.

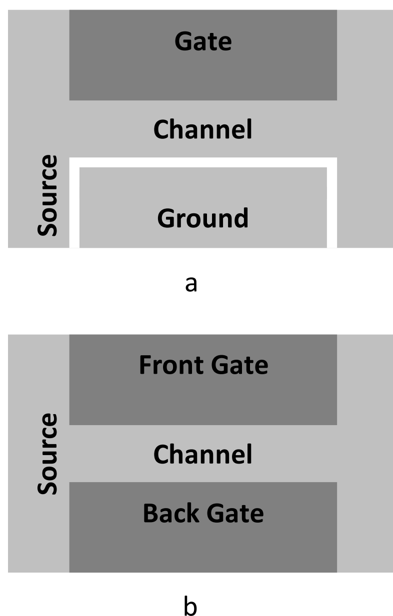
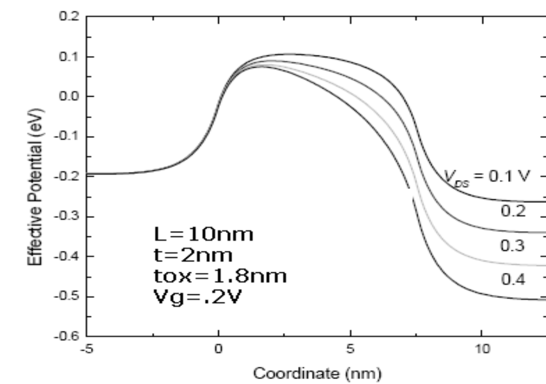


Figure 2.1: The models of (a) single-gate and (b) double-gate nanoscale SOI MOSFETs, used in this study

2.2 SOURCE-DRAIN I-V CURVES

Fig. 2.2 shows typical families of *I-V* curves for both transistors. In both cases, the reduction of the gate length in the single-gate transistors leads to an almost similar suppression of current saturation at larger drain-source voltages. Again, the main difference between the two MOSFET species is that it takes twice more gate voltage to change the current in the single-gate transistor by a certain amount, than in its double-gate counterpart.



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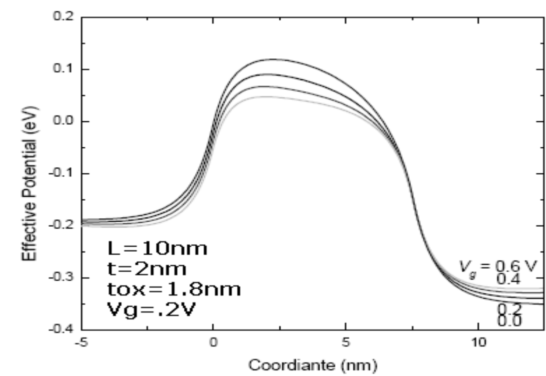

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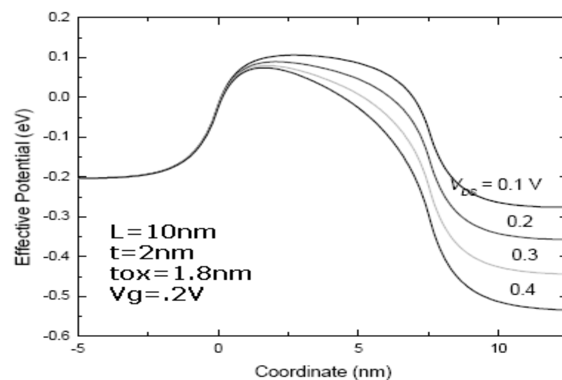

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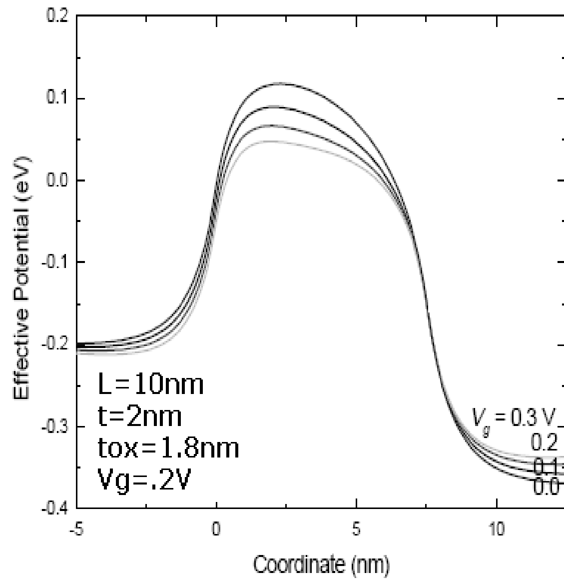


Discussion

It is clear from the results presented in the previous sections that several issues need to be considered when designing an L_G = 10 nm DG MOSFET. The final performance of our model device is summarized in Table 2.2. In order to achieve good short channel characteristics at such small channel lengths, a thin silicon body needs to be used. It has been reported in the literature that a 5 nm body can meet the ITRS-99 specification of I_{OFF} for a channel length of 10 nm [22]. In our study we find that if fabrication uncertainties are considered, the permissible value of body thickness needed to meet the off-current requirement is reduced to 3 nm. For this choice of silicon film thickness, a 10% variation in the gate length along with a single monolayer variation in the body thickness results in a net threshold voltage degradation of ~80 mV. This degradation is ~50% of the nominal threshold voltage. Had a thicker body been used, this variation would be more pronounced as a result of reduced short-channel immunity. It appears that a very high degree of fabrication accuracy will be required to produce such small transistors

RESULT AND CONCLUSION

DEVICE SIMULATION

Electrical characteristics of devices were simulated (using Multi-gate Nanowire FET on http://nanohub.org [22-23]) for the silicon island having width and thickness of 25 nm, while the gate oxide thickness is 1.5nm. Tungsten is used as gate (work function = 4.63 eV), doping concentration in channel is uniform and equal to 1 x 10^{15} cm^3. Simulation is performed for gate lengths L, of 10, 20, 30, 40, 50 & 60 nm. We have used a width of 25 nm, to prevent the electrical field lines from the drain from terminating on the back of the channel region, because of the bottom part of the **π**, **Ω** and GAA

NATURAL LENGTH MODEL

It gives a measure of the short channel effect inherent to a particular device structure. The concept of "natural length", λ represents the extension of the electric field lines from the drain in the channel region [24]. A device is said to be free of short channel effects if the gate length is at least 5-8 nm larger than λ. Suzuki et al [25] has given expression for λ and given by

TRRRRT

$$\lambda = \sqrt{\frac{\epsilon_{Si}}{2\epsilon_{ox}}\left(1 + \frac{\epsilon_{ox}t_{Si}}{4\epsilon_{Si}t_{ox}}\right)t_{Si}t_{ox}}$$

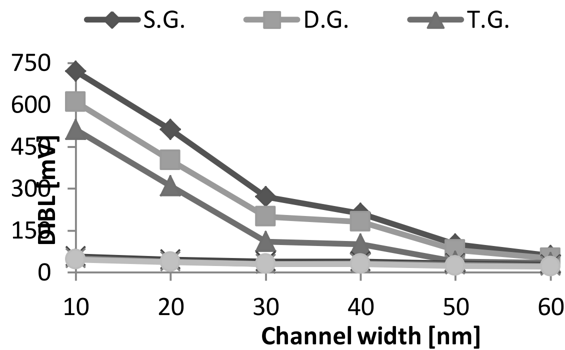
(4.1) Where t_{si}, t_{ox} are the silicon and oxide thickness and ϵ_{Si}, ϵ_{ox} are the permittives of *Si*, and SiO_2. As the expression for generalizing the λ concept to all MuGFETs by writing

$$\lambda_n = \sqrt{\frac{\epsilon_{Si}}{n\epsilon_{ox}}\left(1 + \frac{\epsilon_{ox}t_{Si}}{4\epsilon_{Si}t_{ox}}\right)t_{Si}t_{ox}} \quad (4.2)$$

Where *n* is the effective no of gates, whose value is calculated from the dependence of threshold voltage on silicon film thickness, and its value decrease as the no of gates increases from single gate MOSFETs to GAA MOSFETs because of the increasing influence of the gate over the potential in the channel region.

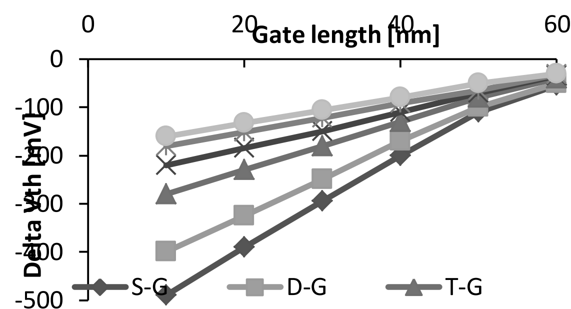
BACK CHANNEL CONDUCTION & DIBL MODEL

As the vertical potential profile underneath a thin-film SOI device is controlled by potential lines originating from the source and drain rather than by the front gate, the potential inside the buried oxide increases linearly with drain bias. This lateral potential coupling from the source and drain causes back-channel conduction and DIBL. Fig. 4.1 (a) & (b) shows the drain-induced barrier lowering effect and the threshold voltage roll-off in fully depleted SOI MOSFETs with different gate structures



different effective gate lengths.

(a)



(b)

Figure : DIBL and threshold channel roll-off in fully depleted SOI MOSFETs with different gate structures and different gate lengths W = T_{Si} = 25 nm, N_A = 1 x 10^{18} cm^3.

The DIBL is defined as the difference in threshold voltage when the drain voltage is increased from 0.1 to 1 V. The threshold voltage roll-off, ΔV_{th}, is defined as the threshold voltage measured at V_{DS} = 0.1V at any gate length minus the threshold voltage at L = 50nm. DIBL is most effectively suppressed by the quadruple-gate structure, but the **Ω** and **π** -gate device comes a close second and third. The reason for less short channel effects in **Ω** & **π** -gate device is that the lower part of the gate sidewalls effectively acts as a back gate through lateral field effect in the buried oxide. Similarly, it can be observed that the threshold voltage roll-off is minimized by the use of the quadruple-gate structure, but the **Ω** & **π** -gate device shows an excellent behaviour as well.

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